MAI in Computer Engineering

Self Tuning Algorithms
Running on Intel's Transactional Memory

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Abstract

As processors grow into a new era where the number of cores on a chip is growing to meet consumer demands for greater performance, we need to utilise new advancements in hardware to meet these demands. Intel have recently released their implementation of Hardware Transactional Memory and using this it is possible to obtain greater performance of multithreaded applications. However, serial data structures do not benefit from these new advancements in the same way as more parallel data structures such as a binary search tree do. Using a technique called Split Transactions it is possible to show considerable performance increases over current state of the art approaches with a serial data structure such as an ordered linked list. The performance increase that is observed by using this method on an ordered linked list can be up to 9 times greater than transactional memory which is not utilising split transactions. Split transactions are also 9 times faster than a conventional lock based approach.